WHAT IS CLAIMED IS:

1. A method of communicating with an embedded microcontroller in a data processing system, comprising:

programmably selecting a plurality of pins of the microcontroller for use as test lines;

receiving a scan command at a first one of the test line pins of the microcontroller;

emulating a virtual scan path through a portion of at least one logical block of the microcontroller with software that is embedded in the microcontroller to access one or more registers in the logical block, in response to said receiving step; and

transmitting scan results at a second one of the test line pins of the microcontroller.

2. The method of Claim 1 wherein said emulating step accesses the one or more registers to thereby change a functional mode of the microcontroller.

3. The method of Claim 1 wherein said emulating step accesses the one or more registers to thereby gather diagnostic information.

4. The method of Claim 1 wherein said receiving, emulating, and transmitting steps are compliant with IEEE standard 1149.1 for a test access port and boundary-scan architecture.

5. The method of Claim 1 wherein the microcontroller assigns a high-priority internal interrupt routine to service test line pin activity.

6. The method of Claim 1, further comprising the step of interconnecting said first and second test line pins with a test bus structure to form a scan ring.

7. A microcontroller comprising:

input/output pins;

a plurality of logical blocks operatively interconnected to said input/output pins;

a memory device; and

firmware instructions stored in said memory device for programmably selecting a plurality of said input/output pins for use as test lines, receiving a scan command at a first one of said test line pins, emulating a virtual scan path through a portion of at least one of said logical blocks to access one or more registers in said at least one logical block, and transmitting scan results at a second one of said test line pins.

8. The microcontroller of Claim 7 wherein said firmware instructions emulate the virtual scan path to access said one or more registers and thereby change a functional mode of the microcontroller.

9. The microcontroller of Claim 7 wherein said firmware instructions emulate the virtual scan path to access said one or more registers and thereby gather diagnostic information.

10. The microcontroller of Claim 7 wherein said firmware instructions receive the scan command, emulate the virtual scan path, and transmit the scan results in compliance with IEEE standard 1149.1 for a test access port and boundary-scan architecture.

11. The microcontroller of Claim 7 wherein said firmware instructions assign a high-priority internal interrupt routine to service test line pin activity.

12. The microcontroller of Claim 7 further comprising a hardware JTAG interface.

13. A data processing system comprising:

at least one processor; and

at least one embedded microcontroller interconnected with said processor, said microcontroller having input/output pins, a plurality of logical blocks operatively interconnected to said input/output pins, a memory device, and firmware instructions stored in said memory device for emulating a dedicated logic function, said firmware instructions further programmably selecting a plurality of said input/output pins for use as test lines, receiving a scan command at a first one of said test line pins, emulating a virtual scan path through a portion of at least one of said logical blocks with software that is embedded in said microcontroller to access one or more registers in said at least one logical block, and transmitting scan results at a second one of said test line pins, while emulating the dedicated logic function.

14. The data processing system of Claim 13 wherein said firmware instructions emulate the virtual scan path to access said one or more registers and thereby change a functional mode of said microcontroller.

15. The data processing system of Claim 13 wherein said firmware instructions emulate the virtual scan path to access said one or more registers and thereby gather diagnostic information.

16. The data processing system of Claim 13 wherein said firmware instructions receive the scan command, emulate the virtual scan path, and transmit the scan results in compliancze with IEEE standard 1149.1 for a test access port and boundary-scan architecture.

17. The data processing system of Claim 13 wherein said firmware instructions assign a high-priority internal interrupt routine to service test line pin activity.

18. The data processing system of Claim 13 wherein said first and second test line pins are interconnected with a test bus structure to form a scan ring which includes said processor.

19. A computer program product comprising:

a storage medium adapted to be read by a microcontroller; and

program means stored on said storage medium for programmably selecting a plurality of pins of the microcontroller for use as test lines, receiving a scan command at a first one of the test line pins of the microcontroller, emulating a virtual scan path through a portion of at least one logical block of the microcontroller to access one or more registers in the logical block in response to said receiving of the scan command, and transmitting scan results at a second one of the test line pins of the microcontroller.

20. The computer program product of Claim 19 wherein said program instructions further access the one or more registers to thereby change a functional mode of the microcontroller.

21. The computer program product of Claim 19 wherein said program instructions further access the one or more registers to thereby gather diagnostic information.

22. The computer program product of Claim 19 wherein said program instructions perform said receiving, emulating, and transmitting in compliance with IEEE standard 1149.1 for a test access port and boundary-scan architecture.

23. The computer program product of Claim 19 wherein said program instructions further assign a high-priority internal interrupt routine to service test line pin activity.